

**Amendments to the Drawings:**

The attached sheet of drawings includes changes to Fig. 2A and the new drawing, Fig. 2B, replaces the original sheet including Fig. 1, 2, and 2A. In Figure 2A, the missing elements 260 on top of the dies are added, and the thickness of elements 260 that contact the substrate 220 is reduced with respect to the chip thickness to depict the embodiment more closely. No new matter is added.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

**Remarks/Arguments:**

Applicant thanks Examiner Ho for his careful examination of this application and clear and detailed explanation of the claim rejections. In response, applicant amends the application as follows:

1. Applicant amends the specification to correct a typographical error. There is no new matter in the amended specification.
2. Applicant amends drawing figure FIG. 2A to depict the invention more clearly. There is no new matter in the amended drawings.
3. Applicant adds new drawing figure 2B following the instruction in ¶3 of the Office action to show two dies operable to fit inside one cavity when the lid is coupled to the substrate as described in the original claim 22. There is no new matter in the new drawing.
4. Applicant cancels claims 1-14, 23, 24, and 35.
5. Applicant amends claim 32 according to the instruction in ¶4 of the Office action to overcome the objection.

Regarding the claim rejections, applicant responds as follows:

1. Regarding the §112 first paragraph rejection against claim 25, applicant respectfully submit that the rejection is improper because this application clearly enables one skilled in the art to make and use the system claimed in claim 25. Claim 25 describes a system that comprises a heat conducting layer that adheres to the lid, contacts but not adheres to the chip. It is well known in the art of integrated circuit device manufacture that, for example, many common solder materials adhere well to metallic surfaces of common heat sinks but do not adhere well to bare silicon surface. Therefore, one skilled in the art can follow the disclosure in this application and select the appropriate material for the lid, the chip and the solder material to make and use the invention described in claim 25.

2. Regarding the §112 second paragraph rejection against 25, applicant again respectfully submits that rejection is improper because claim 25 is clear and unambiguous, and it does particularly point out and distinctly claim the invention. The terms “to contact” and “to adhere” have clearly different definitions and they can be ascertained in any general dictionary. For instance, Webster’s New World College Dictionary defines “to contact” as “the act or state of touching or meeting [two surfaces in contact]”; and “to adhere” as “to stick fast; stay attached”. To apply these definition to claim 25, one can clear understand that the conducting layer sticks fast or stays attached to the inner surface of the cavity; and while the conducting layer touches or meetings the top of the chip, it does not sticks fast or stays attached to the chip.
3. Amendment to claim 15 overcomes the 102(b) rejection against claim 15 over the Atwood reference (US 6,656,770):

The Atwood reference discloses a semi-molten material between the IC chip and its associated heat exchanger to melt and solidify in the IC chip operational temperature range.<sup>1</sup> It does not disclose a system that includes two dies having different thickness, it does not disclose a conductive layer formed such that the thickness of the first die and the conductive layer on top of on top of the first die being substantially equal the thickness of the second die and the conductive layer on top of the second die.

Because the Atwood reference fails to disclose all the limitations of claim 15, it does not anticipate claim 15 and claim 15 stands patentable over the Atwood reference.

Claims 16-19 depend directly on claim 15 and stand patentable over the Atwood reference at least by virtue of their dependency.

4. As amended, claim 25 overcomes the 102(e) rejection over the Sur reference (US 6,724,078):

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<sup>1</sup> US 6,656,770, col. 1, ll. 16-18.

One element of limitation in claim 25, as amended, is heat conducting layer that conforms to the surface contour of the chip, comes in contact to the top surface of the chip and; but not adhere to the chip. Contrarily, Sur teaches depositing an “adhesion metal layer” directly to the top of the chip. In the following paragraphs, Sur discloses the preparation of the chip back surface and deposition of an adhesion layer of metal:

... Before deposition of the one or more metal layers 82, 84, and/or 86, the wafer surface can be prepared with a sputter etch, if desired, to improve the adhesion of the adhesion layer 82 to the die surface; however, a sputter etch is not essential. Nor is the condition of the wafer surface essential. The wafer surface can be in unpolished, polished, or back-ground form.

Next, an adhesion layer 82 of a metal that adheres well to silicon, silicon oxide, or silicon nitride, such as titanium (Ti), is deposited onto the etched surface. In one embodiment, a 500 Angstrom layer of titanium is sputtered onto the etched surface. Chromium (Cr), vanadium (V), and possibly zirconium (Zr) could be substituted for Ti.<sup>2</sup>

This adhesion layer clearly “adheres” to the wafer surface because it is well known in the art of integrate circuit device manufacturing that a layer of metal such as Ti, Cr, V, or Zr, when deposited on the back of silicon surface, readily forms a layer of inter-diffused metal-silicon layer. This enhances the adhesion of the metal layer to the die surface; while the conducting layer in claim 25 touches or meetings the top of the chip but not sticks fast or stays attached to the chip.

The system in another embodiment of this application does include a binding layer to glue the lid to the chip to form a bond. However, the system described in claim 25 limits the system to a state where the conducting layer contacts but not adhere to the chip. This limitation clearly distinguishes claim 25 over the Sur reference.

Claims 28 – 31 and 33 depend directly on claim 25 and include all the limitations in claim 25, because Sur does not anticipate claim 25, the reference does not anticipate claims 28 – 31 and 33.

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<sup>2</sup> US 6,724,078, col 4, l. 65 – col. 5, l. 10.

5. The Baek reference (US 6,756,668) does not anticipate claim 25, or render it obvious. The Baek reference discloses a semiconductor package that includes a thermal interface material (TIM) with voids to reduce thermomechanical stresses.<sup>3</sup> The formation of the TIM and the voids is described as follows:

Referring to FIGS. 3 and 4, in order to form the voids 180, a patterned layer 170 is formed between a back surface of the CPU chip 120 and the thermal interface material 160. The patterned layer 170 comprises void pads 176, a copper pattern layer 172, and a nickel/gold plating layer 174. The void pads 176 are preferably made of a material (such as a photo solder resist (PSR) film and a polyimide tape) that is non-wettable by solder. The void pads 176 can be arranged substantially uniformly along the perimeter of the back surface 123 of the CPU chip 120. The copper pattern layer 172 covers the back surface 123 of the CPU chip 120 except for areas in which the void pads 176 are formed.<sup>4</sup>

It is clear from the description that the portion of the TIM closest to the chip includes a copper layer 172 interlaced with a void pattern 176 formed of material such as photo solder resist or polyimide tape. It does not disclose a heat conducting layer that conforms to the surface contour of the chip, comes in contact to the top surface of the chip and; but not adheres to the chip. Therefore, the Baek reference does not anticipate claim 25.

Because claims 28 – 31 and 33 depend directly on claim 25 and include all the limitations in claim 25, the Baek reference does not anticipate claims 28 – 31 and 33.

6. Because Baek fails to disclose at least the limitation as noted in the previous paragraph and it does not suggest combining such a limitation, it can not render claim 25 obvious.

Because claims 28 – 31 and 33 depend directly on claim 25 and include all the limitations in claim 25, and because claim 25 is not obvious over the Baek reference, claims 28 – 31 and 33 are not obvious over the Baek reference.

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<sup>3</sup> See, US 6,756,668, Abstract.

<sup>4</sup> Ibid, col. 3, ll. 47-56.

7. Claims 20 and 21 can not be obvious over the Wilson reference (US 2004/0000712 A1) because Wilson does not render claim 15 obvious and claims 20 and 21 depend directly on claim 15.
8. Claim 32 can not be obvious over the Sur reference in view of the Wilson reference because both the references separately in combination do not render claim 25 obvious and claim 32 depends directly on claim 25.
9. Claim 15 can not be render obvious over the Sherif reference (US 5,623,394) in view of the Rumer reference (US 2003/0178730) because neither reference discloses all the limitations in claim 15 and there is no suggest combining all the elements in claim 15:

Claim 15, as amended, limits the system to include at least two dies that are different in thickness and a conductive layer on the top of the dies such that the thickness of the first die plus the conductive layer on the top of the first die substantially equals the thickness of the second die plus the conductive layer on top of the second die.

Contrarily, the Sherif reference discloses an apparatus for cooling chips by using different thermally conductive materials and cavities of different depths. It does not disclose dies of different thickness and varying the conductive layer thickness to compensate for the difference. This deficiency is not cured in the Rumer reference because the Rumer reference does not teach multiple dies.

Because both the Sherif reference and the Rumer reference fail to disclose all the limitations of claim 15 and there is no suggestion to combine all the limitations, claim 15 is not rendered obvious over the references.

Because claims 17 – 19 and 22 depend directly on claim 15, they too must not be obvious over the references.

10. The Edwards reference (US 5,819,402) does not render claim 25 obvious in view of the Rumer reference because Edwards does not teach all the limitations in claim 25 and the Rumer reference does not cure the deficiency:

As explained in a previous paragraph regarding the 102 rejection over the Sur reference, claim 25 limits the heat conducting layer to conform to the surface contour of the chip, to come in contact to the top surface of the chip and; but not to adhere to the chip.

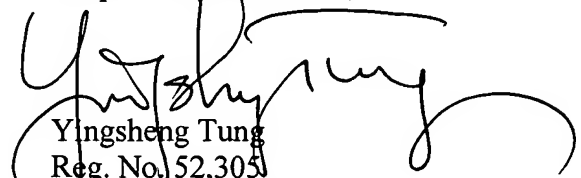
Applying again the ordinary definition of “to contact” and “to adhere”, it is clear that Edwards fails to teach a heat conducting layer that contacts but not adheres to the chip. In Edwards, the material that sits between the chips (51, 52, 53, 54, and 55) and the cap or cover (50) is a thermal paste (71). It is well-known in the art of integrated circuit device manufacturing that thermal pastes are designed to adhere well to the chips. The Rumer does not cure this deficiency because it too, specifically teaches a phase change thermal interface material that “adheres to the surface”.<sup>5</sup>

Because the Edwards reference does not disclose all the limitations in claim 25 and the Rumer reference fails to cure this deficiency and because neither reference suggests combining all the limitations in claim 25, claim 25 is not rendered obvious over the references.

Because claims 24 – 31 and 33 depend directly or indirectly on claim 25, they must not be obvious over the references.

In summary, applicant respectfully submits that, as amended, this application is in allowable form and the claims in the amended form distinguish over the cited reference and are therefore patentable over the references. Applicant respectfully requests that this application be further examined and the pending claims timely pass to allowance.

Respectfully submitted,

  
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<sup>5</sup> See, US 20030178730, [0017] and [0027].

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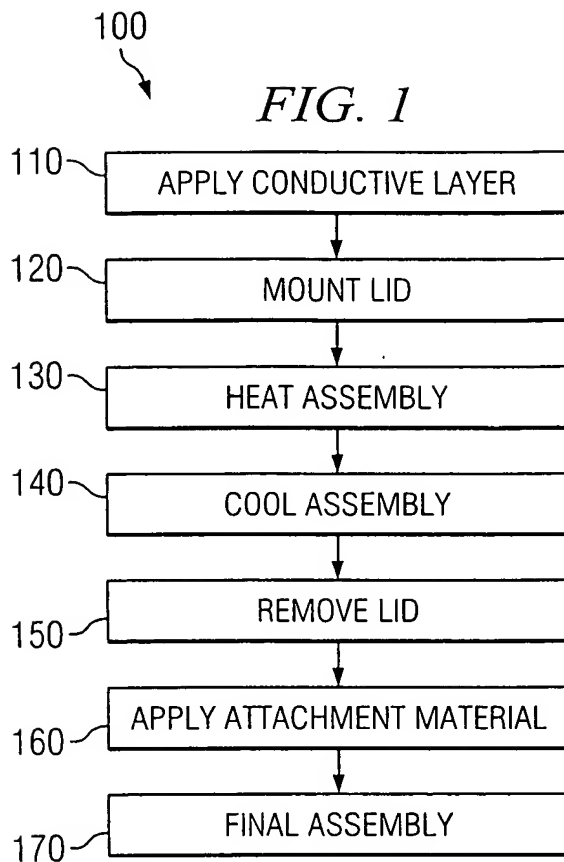


Fig 2B added

